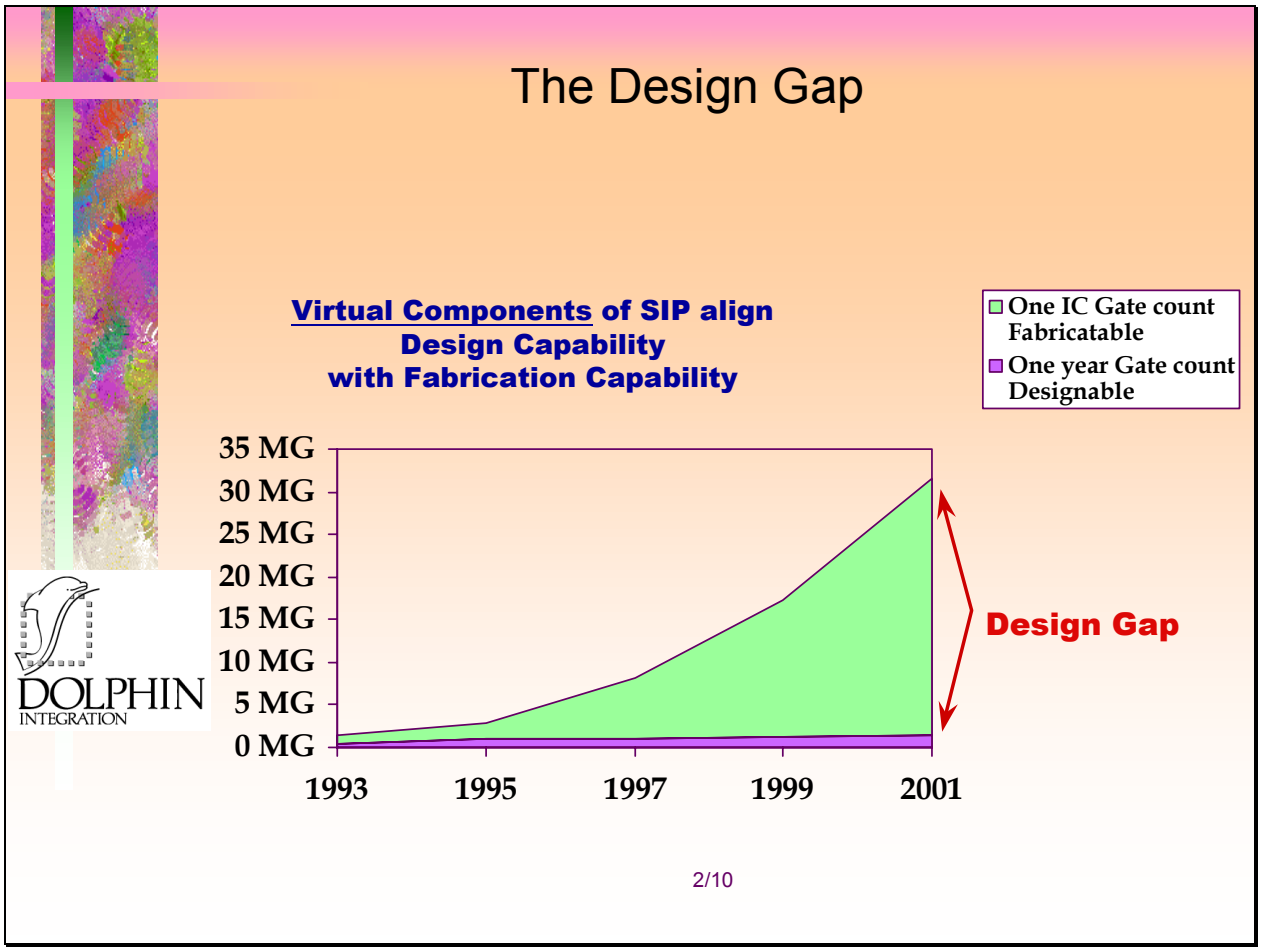
Challenges in mixed-signal design for the SoC era

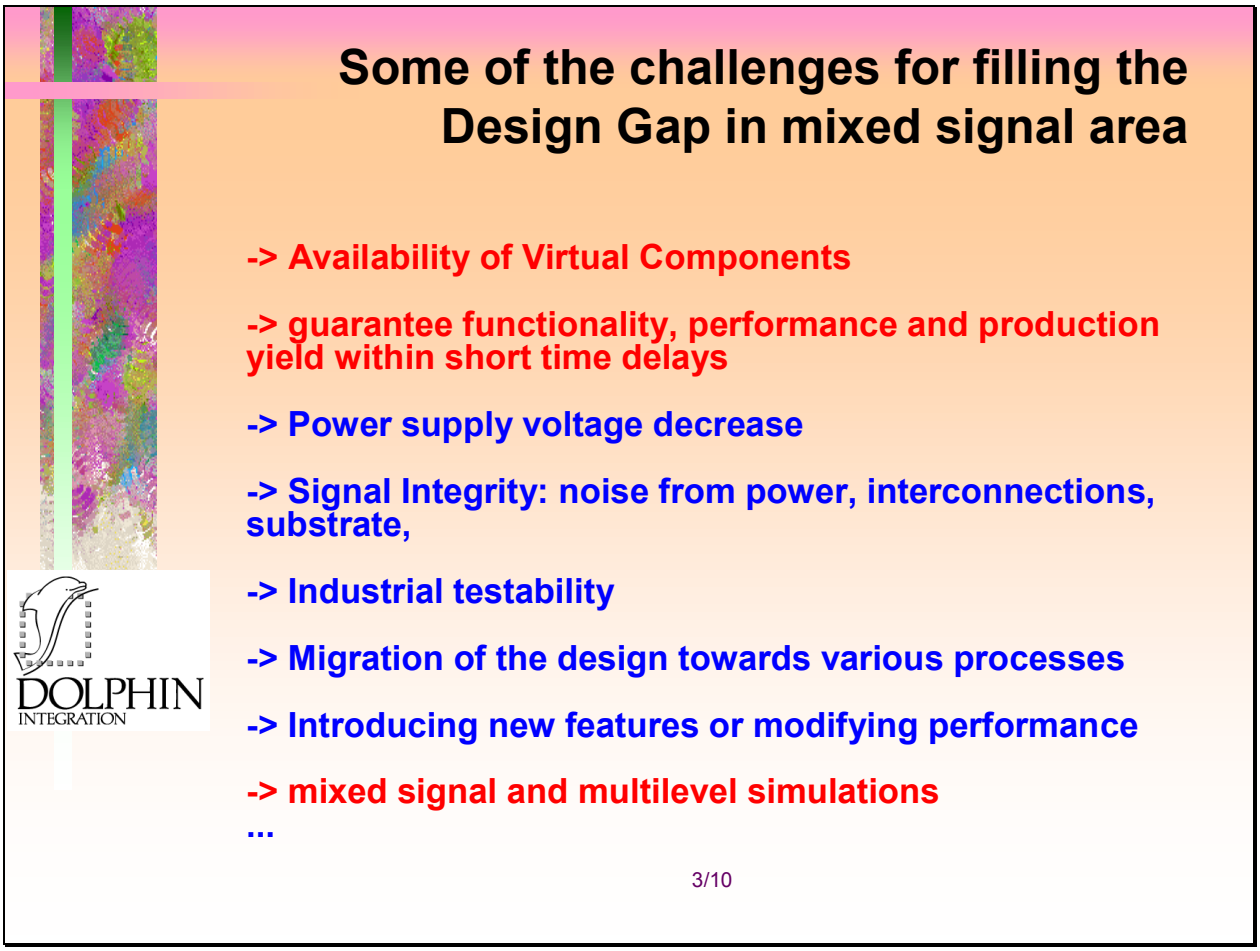
DATE 2001

by Jean-François Pollet, Chief Operating Officer

I am representing Dolphin Integration, a 130 people company specialized in microelectronics design and offering products and services to our customers in two domains:
- the virtual components, sometimes called IP blocks; among our specialties having an interest for this panel are mixed signal Virtual Components like ADCs, DACs, PLL but also embedded memory generators
- the enabling technologies and more specifically in the frame of this discussion, a mixed-signal simulator named SMASH
Mixed-signal challenges for the Soc era!
The title is impressive especially when Georges tells you: you have five minutes to make a short introduction on this issue.
I will do my best!
Let us present this stuff through the “Design Gap”



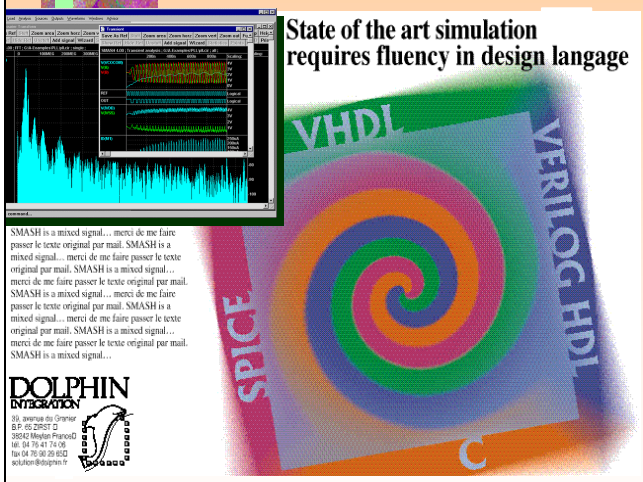
This graphic is now well known but represents a good summary of the challenges for the current and future IC designs.
No team with human size could expect to design from scratch in a decent project duration (say one year) more than about a million gates. Meanwhile, the economic size of an integrated circuit can house more than twenty-five times that amount of design.
Such a "Design Gap" constitutes a threat and a challenge for reassessment of the design paradigm in the IC world.
To benefit from the fabrication capability, this challenge has to be addressed by two complementary offerings: the use and re-use of Virtual Components, and the capability of EDA tools to design such complex Integrated Circuits
Our question to be debated in this panel is: what is specific for the mixed signal area?



There are some paradoxes in the SoC industry. Here is the crux of the matter for the analogue and fast electrical parts: Innovative products involving SoC development often require usage of the latest technological process, together with a mix of high performance logic and analogue functions.
Reducing cost, time and risk of SoC designs requires the re-use of Virtual Components. Re-use clearly means that such functions have already been used and this is the paradox when analogue parts are involved because analogue functions are always different from one application to another one and they have to be retargeted and tuned for each process.
On the logic side, HDL languages offer the possibility for designing complex logic functions while remaining independent from the technological fabrication process until an advanced stage in the SoC design flow.
But analogue functions (or high speed logic functions) have to be delivered as hardware VCs, because their performances can be guaranteed only after careful tuning and checking through detailed design rules and transistor characteristics of the targeted process.
All these issues, specific to the Analog and mixed signal world, add to the usual SoC design flow new challenges listed on the slide:
-> to guarantee functionality, performance and production yield within short time delays
-> to cope with power supply voltage decrease
-> Evaluate the impact of noise on analog performances
-> Take into account the industrial testability
-> To be able to quickly migrate a design towards various processes while introducing new features or modifying its performance
- > the capability of doing efficient mixed signal simulations all along the design process.

All these requirements have to be fulfilled with a high level of quality implying bug-free, reliable solutions and high production yields.

Capability of mixed signal simulations all along the design process

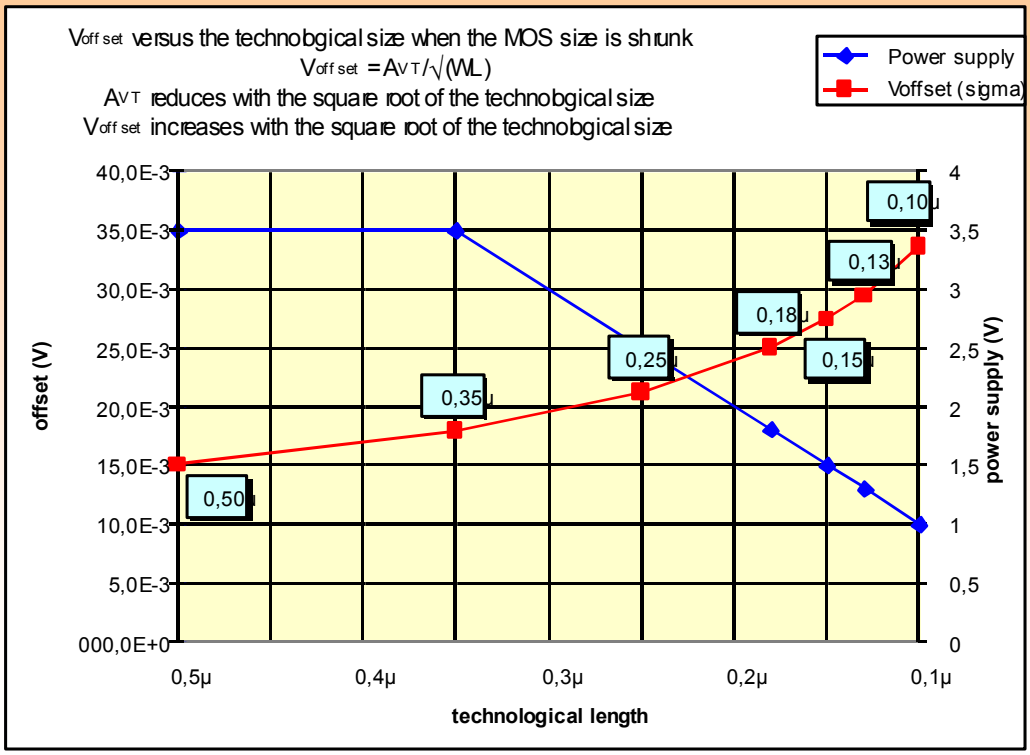


- Single kernel Mixed Signal: **logic + analog**
- Multi-Level Simulation: **Behavioral + Gate + Electrical**
- Multilingual: **SPICE, Verilog-HDL, C and VHDL**
- Virtual Test and Diagnostic with **VHDL-AMS** for SoC tesbenches
- Multi-solver/model simulation engine **BSIM1, 3v3, EKV, Level 1-3, MM9, TRANS…**
- Openness to any data capture **Composer, SCS, ...**
- Available on all platforms **Unix/Solaris or Windows** and soon **Linux**
- **MEMS** and POWER modeling through ABCD and **VHDL-AMS**

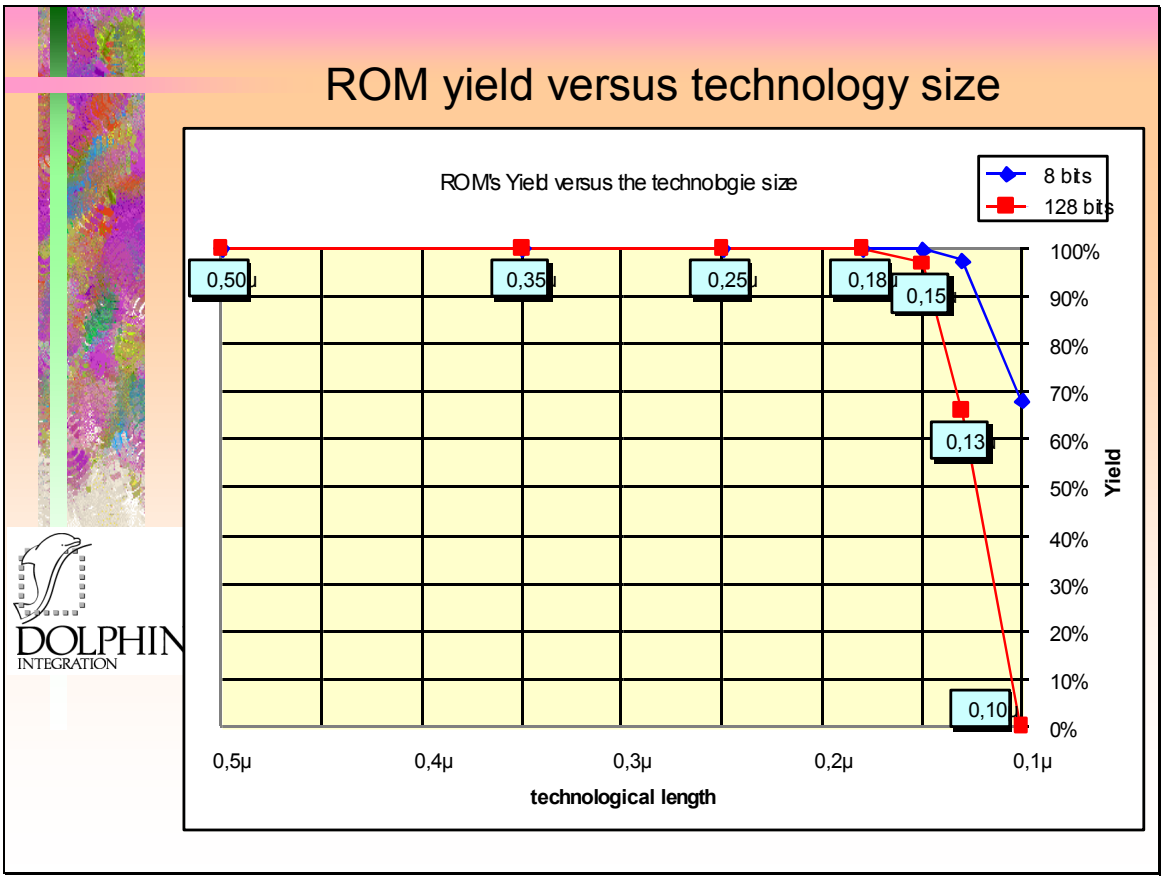
4/10

I will concentrate briefly on two other issues which are of highest importance
-> the first one is to have the capability of doing efficient mixed signal simulations all along the design process.
This is true for the development of virtual components as well as for the development of SoCs embedding mixed signal functions.
In this area we and our customers are currently using our simulator SMASH whose main features are listed on the slide.
Thanks to the usage of standard languages like VHDL, SPICE, Verilog, every user can use and re-use blocks coming from different sources, put them together and simulate the overall function.
Thanks to the multi-level capability, the designer can choose for each of these blocks the right level of accuracy he needs. The level of accuracy depends on the step of the design, starting from electrical simulations for basic blocks to behavioral modelling for checking the interactions between blocks.
Various levels may be combined together.
SMASH has been the first simulator of the market providing VHDL-AMS simulation capability. Such simulations are paramount for the simulations of complex design embedding analog and logic functions.

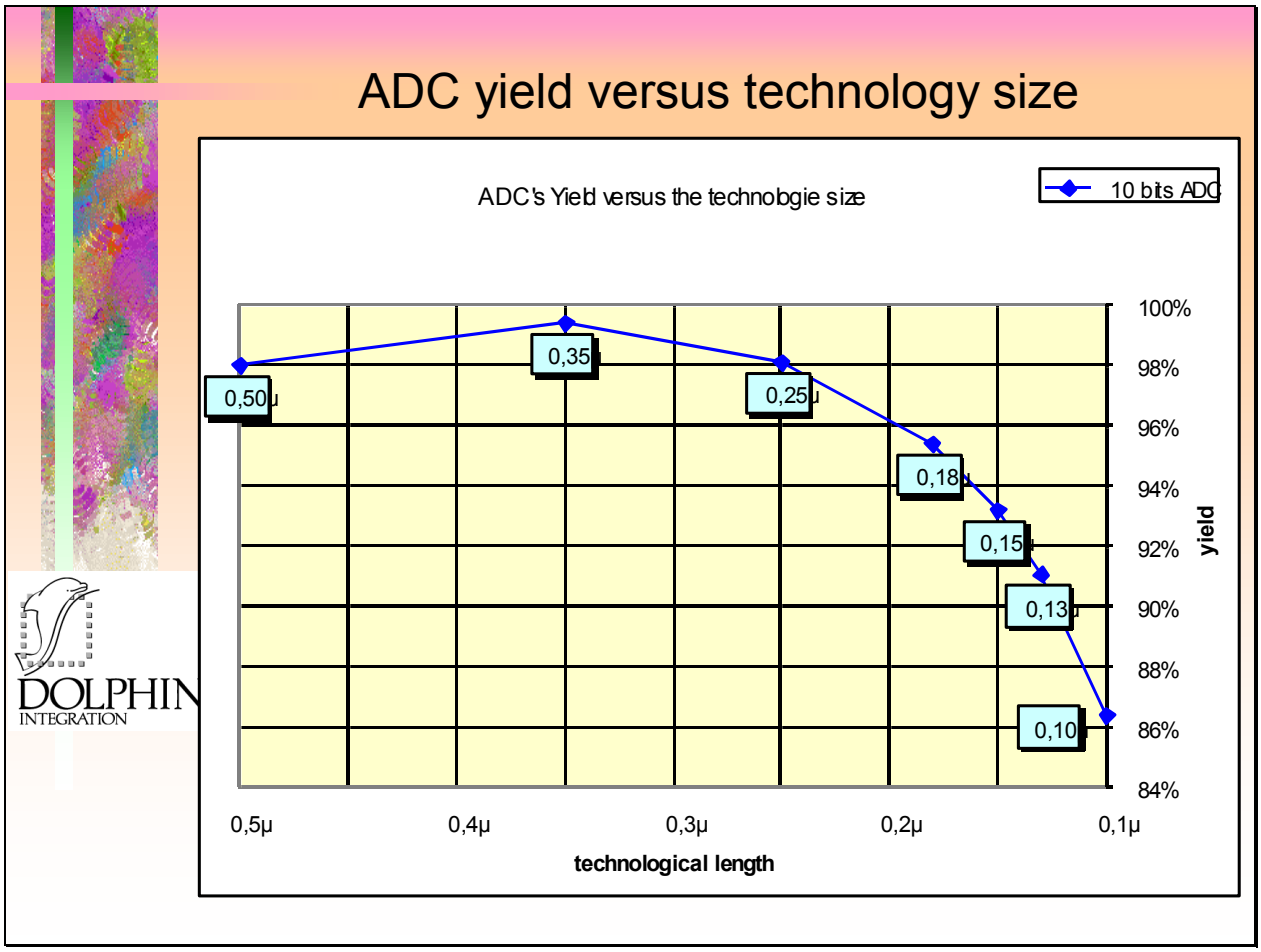
One example: MOS matching versus technology size



-> the second topic I will briefly describe is the capability to guarantee functionality, performance and production yield within short time delays. More precisely I will mention one of the critical points designers will have to face with the very deep sub-micron processes: the evolution of MOS matching with the technological processes and its consequences on production yield.
On the slide we have represented the variation of MOS matching, when a design is shrunk from a technological process of a generation to a new generation.
Two cumulative effects are shown: the power supply voltage, decreasing with each process generation and the matching value, increasing with each process generation. The results have been computed with 1 sigma values, but the effect would be greater with 3 sigma or more.
The ratio between the offset value and the power supply voltage is multiplied by 5 from a 0.35 µm to a .12 µm process. As a consequence, every schematic sensitive simultaneously to offset and supply voltage will be deeply affected.
The next two slides illustrate the effect of matching on the yield of an embedded ROM generator and on a 10 bits ADC



You can easily compute the effect of transistor matching on the yield of a ROM memory generator when you consider that one of the more sensitive cells of a memory is the read amplifier.
For a given read margin, the yield will decrease when the offset will increase.
The slide shows what happens to the yield when we start from a design initially optimized for a 0.5 µm or 0.35 µm process when we apply a migration based on a skrink without re-designing the basic cells.
The drastic increase of offset values with very deep sub-micron processes results in a very fast decreasing yield, not acceptable at all. Notice that the more read amplifiers you have, the more the yield is decreased which seems quite obvious.
What does all this stuff mean?
- First, the impact of offset is paramount for very deep sub-micron processes requiring a lot of care for the design
- Second and the most important in the frame of this panel is that EDA tools must be provided to help the designer to evaluate the impact of such offsets. Monte Carlo simulations are not sufficient for helping the designer improve its design.



OK, but you will tell me that memories are not analog. It's less and less true. With VDSM processes, even digital circuitry become analog. But look at the following slide showing a different approach for migrating a design from one process to another one.
The assumption here is that we keep the same dimensions for the transistors when we migrate from one process to another one. This methodology is sometimes used in analog, when the silicon area of a block is not of major importance; the drawback is that you do not benefit from the higher density offered by the new processes. Another assumption is that the migration from a process to the next one is made without shrink and the reference voltage is linear with the power supply voltage.
The yield decreases with each process generation and becomes significant for VDSM processes.
The consequence is that when you cumulate every possible effect in a SoC embedding analog blocks and embedded memories, the yield losses are multiplied and the result may be dramatic. 10% of yield loss for two independent functions will result in a 19% overall yield loss.
The requirements are the same as previously mentioned: EDA tools must provide solutions for helping the designer to evaluate such yield loss.

The solution!

-> Yield loss prediction thanks to a powerful simulation methodology

-> Applicable to design critical issues like devices matching, parameters dispersions, …

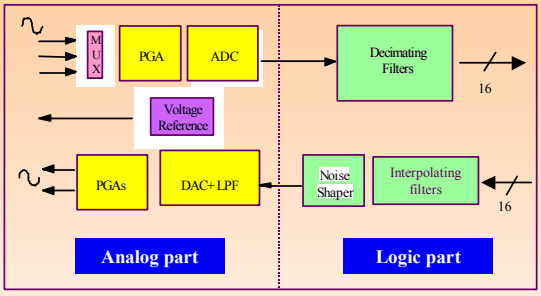
Available in the next release of SMASH simulator

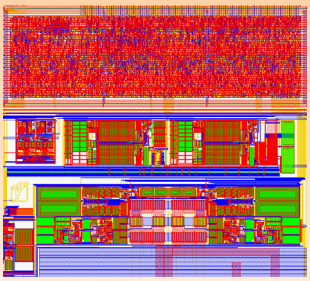
I see some of you becoming anxious because they are thinking to the tape-out they have done last week, just before coming to this conference; be reassured, anxiety in IC design is the beginning of wisdom.
More seriously, is there a solution?
As specialists in mixed signal designs in our Company, we have always be sensitive to offset effects on production yield and we became aware of the strong impact of transistors matching in very deep sub-micron with the migration of some of our Virtual Component towards such processes.
Development teams including IC designers and software designers have worked together to find a solution to this issue. The solution has been found, tested on our own designs and is currently in a patenting process.
It will be incorporated in the next version of our Simulator.
Thank you for your attention.

Example of a mixed-signal ViC

16-bit delta-sigma Analog Front End

Fax, Modem or Audio applications





DOLPHIN INTEGRATION

-> Typically 80 dB THD and SNR

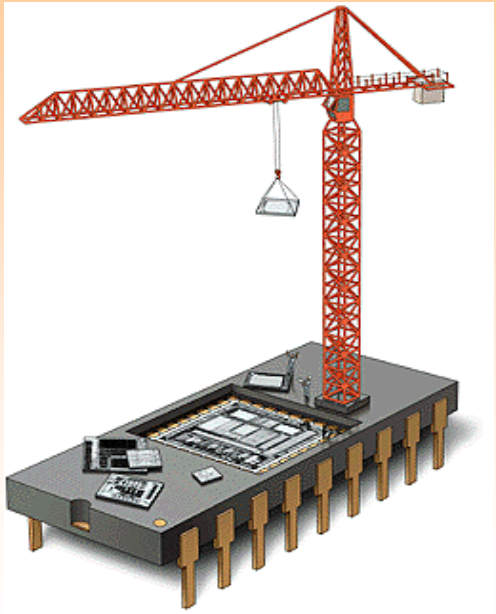
-> Architecture and cells designed for ensuring a safe and fast migration towards any deep sub-micron CMOS 3.3 V processes

-> Deliverables: GDSII, Verilog, specifications, user guide (VSIA recommendations)

9/10

There are some paradoxes in the SoC industry. Here is the crux of the matter for the analogue and fast electrical parts: Innovative products involving SoC development often require usage of the latest technological process, together with a mix of high performance logic and analogue functions.
Reducing cost, time and risk of SoC designs requires the re-use of Virtual Components. Re-use clearly means that such functions have already been used and this is the paradox when analogue parts are involved because analogue functions are always different from one application to another one and they have to be retargeted and tuned for each process.
On the logic side, HDL languages offer the possibility for designing complex logic functions while remaining independent from the technological fabrication process until an advanced stage in the SoC design flow.
But analogue functions (or high speed logic functions) have to be delivered as hardware VCs, because their performances can be guaranteed only after careful tuning and checking through detailed design rules and transistor characteristics of the targeted process.
All these issues, specific to the Analog and mixed signal world, add to the usual SoC design flow new challenges listed on the slide:
-> to guarantee functionality, performance and production yield within short time delays
-> to cope with power supply voltage decrease
-> Evaluate the impact of noise on analog performances
-> Take into account the industrial testability
-> To be able to quickly migrate a design towards various processes while introducing new features or modifying its performance
- > the capability of doing efficient mixed signal simulations all along the design process.

All these requirements have to be fulfilled with a high level of quality implying bug-free, reliable solutions and high production yields.



DOLPHIN INTEGRATION

10/10

There are some paradoxes in the SoC industry. Here is the crux of the matter for the analogue and fast electrical parts: Innovative products involving SoC development often require usage of the latest technological process, together with a mix of high performance logic and analogue functions.
Reducing cost, time and risk of SoC designs requires the re-use of Virtual Components. Re-use clearly means that such functions have already been used and this is the paradox when analogue parts are involved because analogue functions are always different from one application to another one and they have to be retargeted and tuned for each process.
On the logic side, HDL languages offer the possibility for designing complex logic functions while remaining independent from the technological fabrication process until an advanced stage in the SoC design flow.
But analogue functions (or high speed logic functions) have to be delivered as hardware VCs, because their performances can be guaranteed only after careful tuning and checking through detailed design rules and transistor characteristics of the targeted process.
All these issues, specific to the Analog and mixed signal world, add to the usual SoC design flow new challenges listed on the slide:
-> to guarantee functionality, performance and production yield within short time delays
-> to cope with power supply voltage decrease
-> Evaluate the impact of noise on analog performances
-> Take into account the industrial testability
-> To be able to quickly migrate a design towards various processes while introducing new features or modifying its performance
- > the capability of doing efficient mixed signal simulations all along the design process.

All these requirements have to be fulfilled with a high level of quality implying bug-free, reliable solutions and high production yields.