

Guidelines for Verilog-A Compact Model Coding

Gilles DEPEYROT, Frédéric POULLET, Benoît DUMAS DOLPHIN Integration

June 2010

Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany



Outline



Dolphin

- EDA Solutions by Dolphin
- Overview of SMASH
- Context & Goals
- Verilog-A for Compact Modeling
 - Benchmark of Verilog-A vs. SPICE
 - Verilog-A Limitations (for Compact Modeling)
- Recommendations
 - Subset of Verilog-A for Compact Models
 - Focus on Spice integration
- Conclusion and Perspectives

June 2010











A strong synergetic potential between

Silicon Intellectual Property Products

- Embedded memories SRAM, ROM
- Standard cell libraries, low power, high density
- Mixed signal ADC, DAC
- Power management
- 8b, 16b microcontrollers

- EDA Solutions

- Delegation Services
 - Four professions in growing demand for design in microelectronics
- Turnkey SoC Design
 - low power, mixed signal ASICs
- Since 1985, now 180 including 145 engineers
- On Alternext stock-market
- 11 M€ sales turnover









EDA Solutions by Dolphin



SLED – Schematic Link Editor



SMASH[™] – Mixed-Signal Multi-Language Simulator



SCROOGE – Mixed-Signal Power Consumption Estimator – Powered by SMASH[™]



SoC GDS – Layout Analyzer & Processor







Overview of SMASH

File Edit Setup Probes Analysis Debug Waveforms Processing Results Tools Windows Help

SMASH 5.12.1

- Mixed-signal
 - Analog
 - Logic
- Multi-language
 - SPICE (including flavors)
 - Verilog
 - VHDL
 - Verilog-A
 - VHDL-AMS
 - C
- Multi-level
 - Structural / Gate
 - RTL
 - Behavioral
- Multi-platform
 - Windows & Linux

- * N (X & & B & 4 ~ ~ O Q Q E E # + + + ? 🕏 泰原語 中 作力作得得 ノル信 回回回回 シ 山本本 山液 📮 -E M4 - CP C:\Program Files\Dolphin\Smash5121\examples\... -C MS-ON -E M6-CP = 99.84ns, dt = 99.84ns, y = 2.1906V, dy = 2.1906V, frequency = 10.0 inl => X. in2 => ¥. -E M7-CP 100n 120n 140n 16 out1 => PHICOT); -E M8-CP - R1 - DEFAULT + RD1 - DEFAULT hufl: hufg generic map(lns,lns) + RD2 - DEFAULT port sap(inl => C, -0- VDD - DC O WREF - DC out1 => COUT); 13 XMHOL - PLL MHOL תחתחתחתחת BUF1 - BUFG end structural NANDS - NANDG PHIOUT NANDA - NANDG NANDS - NANDG > SPICE NANDED - NANDE NOTO - NOTG NOTL - NOTG · vhdl entity instantiation Xwhd1 D PHIOUT FIL_WHDL(STRUCTURAL) -I+ C1 - DEFAULT voor H H H L M K · Low-pass filter R1 PHIOUT WCOCOM 10K SWHOL NAND4 JNI C1 VCCCCM 0 10p STATIC NAMES INC. 0 SWHOL NAND4.OUTL L * Voltage Controlled Oscillator M1 B A O O cn v-Su M2 B A IVDD VDD CD w=10u 1=2u N1 C B on magn 🚑 Browser 📄 Files 🚺 Circuit D Cutput D pl spice vhd.rpt 🕱 Debug D pl spice vhd.log Signal NUMBER OF A DESCRIPTION on signal XMDL.COUT DEXMOLINANDA INZ (XVHDL/REAR) LOG In XIHOL NAND4, "nand whd" line 22 SWHOL NANDH OUTS (WHOL.Y) LOS in XMHDL NAND4, "nand vhd" line 20 User watches Expression watches Local watches Events Breakpoints Backtrace
- Wide range of integrated Compact Models
 - BSIM3, BSIM4, EKV2.6, EKV3, ACM, PSP, VBIC, HICUM, MEXTRAM, MM9...
- Since 1989...



Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany



se wait, or hit ESC to cancel radiated

In 6. Cold





Dolphin's Experience Integration of Compact Models

- ...since 1989
- More than 85 SPICE and mixed models
- 29 MOS models, 5 bipolar • models, 5 diode models, 2 JFET models
- SPICE flavor handling
 - compatibility with competitor specificities (HSPICE, ELDO, PSPICE...)
- **Hierarchical approach**
 - Diode or resistor models called by MOS models
 - Common parameters or functionalities (geometry, diode, noise, matching, documentation...)
- C interface
 - BSIM4, BSIM3, MM11, MM9, EKV2...
- Verilog-A with ADMS XML
 - PSP, EKV3, Juncap2, HICUM

Dolphin Integration

Help: m_models_model_psp1	02_2.dll.htm PSP102 (n	elease 5.13.0d2 of Ma	r 12 200	9)				
II 夺 仓 仓 · · · · · · · · · · · · · · · · ·								
Contents Index Search Instance Parameters: parsed and available with 'IN (<instance_name>.<parameters) '="" function:<="" td=""></parameters)></instance_name>								
(bookmarks) 🔽 📲 🗶	Parameter Name	Default Value	Unit	Description				
	M	1		Parallel multiplicity				
SPICE Models				FATAL ERROR if less than or equal to 0				
E - Capacitors	NP	1		alias of M				
E - Voltage Controlled Vc	II.			Width for M=1				
🐵 🔖 F - Current Controlled Cu		model."		FATAL ERROR if less than or equal to 0				
🕀 🕎 G - Voltage Controlled Cu	T.	MODEL : L	m	Length				
H - Current Controlled V(FATAL ERROR if less than or equal to 0				
J - Junction FET Transist	AS	10	m^2	Bottom area of source junction				
🗉 🔖 K - Inductor couplings 📃 🗕				FATAL ERROR IT less than U				
🗉 🔖 L - Inductors	AD	1p	m^2	Bottom area of drain junction				
M - Mos Transistors				PATAL ERROR II IESS THAN U				
m_models: model lev	PS	1u	m	Perimeter of source junction				
m_models: model_lev				PATAL ERROR II less tianto				
m_models: model_lev	PD	1u	m	Perimeter of drain junction				
m_models: model_ek								
m_models: model_re	GNOISE	MODEL: GNOISE	-	Noise gain				
m models: model mr	NF	1		Number of fingers				
m_models: model_mr			_	WARNING and set to default if less than 1				
m_models: model_an	SA	0	m	Distance between OD-edge and poly from one side				
m_models: model_st:	SB	0	m	Distance between OD-edge and poly from other side				
m_models: model_mr	SD	0	m	Distance between neighbouring fingers				
m_models: model_ps			-i	Integral of the first distribution function for scattered well dopants				
m_models: model_ps	SCA	0		FATAL ERROR if less than 0				
m_models: model_bs			1	Integral of the second distribution function for scattered well donants				
m_models: model_bs	SCB	0		FATAL ERROR if less than 0				
m models: model bs		-		Integral of the third distribution function for scattered well dopants				
m_models: model_bs	SCC	0		FATAL ERROR if less than 0				
m_models: model_bs	sc	0	m	Distance between OD-edge and nearest well edge				
m_models: model_bs	DELVITO	0	V	Threshold voltage shift parameter				
m_models: model_bs	000010	•		Zene Auld weletilte and Gester				
m models: model ek	FACTUO	1		EATAL ERROR if less than 0				
m_models: model_ek								
m_models: model_ek	ABSOURCE	1p	m^2	EATAL ERROR If less than 0				
m_models: model_ek								
m_models: model_ek	LSSOURCE	1u	m	EATAL ERROR if less than 0				
R - Resistors			-	Cata-ordea longth of courses is notion				
🗉 🔖 S - Laplace	LGSOURCE	1u	m	FATAL ERROR if less than 0				
🗉 🧙 T - Lossless Transmission 🚽 –			-	Pottom prop of drain junction				
U - Lossy Transmission Li	ABDRAIN	1p	m^2	FATAL ERROR if less than 0				
V - Voicage Sources Y - Mixed Macromodels			1	STI-edge length of drain junction				
	LSDRAIN	1u	m	FATAL ERROR if less than 0				
			-	Gate-edge length of drain junction				
	LGDRAIN	1u	l m					



Meylan - France **Dolphin Integration GmbH Duisburg** - Germany



Context & Goals

- What needs to be done so that Verilog-A can become the standard for CM coding?
 - Benchmarking performed to understand current status and provide guidelines
 - Guidelines put together for CM coding
- What is at stake?
 - Fully taking into account SPICE-like integration of Verilog Compact Models in the ecosystem
 - Providing a viable and open alternative to "controlled" initiatives (such as TMI or CMI)







Benchmark of Verilog-A vs. SPICE Conditions



Test bench:

- Configurable CMOS delay (400, 4k or 40k MOS)
- Use default values for the parameters of the MOS models
- Use two models, one PMOS and one NMOS
- Computed iterations 2550±5
- Use TRAP method for integration

June 2010

Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany





Benchmark of Verilog-A vs. SPICE Memory × 3

Memory usage (Mb)		SMASH 5.15*		Simulator B		Ratio
		SPICE	Verilog-A	SPICE	Verilog-A	/ SPICE
	Circuit #1	40Mb	51Mb	15Mb	18Mb	1.20
PSP Model	Circuit #2	57Mb	115Mb	47Mb	97Mb	2.06
	Circuit #3	216Mb	633Mb	330Mb	854Mb	2.93
	Circuit #1	39Mb	51Mb	NA	18Mb	0.46
EKV3 Model	Circuit #2	51Mb	116Mb	NA	66Mb	1.29
	Circuit #3	170Mb	807Mb	NA	540Mb	3.18

* The SMASH graphic user interface consumes 34Mb out of the total memory consumption.

June 2010

Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany





Benchmark of Verilog-A vs. SPICE Loading Time × 5

Loading time (seconds)		SMASH 5.15		Simulator B		Ratio
		SPICE	Verilog-A	SPICE	Verilog-A	Verilog-A / SPICE
	Circuit #1	0.25s	1.00s	0.06s	0.75s	12.5
PSP Model	Circuit #2	0.40s	2.28s	0.25s	1.75s	7
	Circuit #3	2.60 s	25.29s	3.24s	10.75s	4.1
	Circuit #1	0.23s	0.51s	NA	0.20s	0.9
EKV3 Model	Circuit #2	0.44s	1.93s	NA	0.74s	1.7
	Circuit #3	2.34 s	21.40s	NA	11.87s	5.1



Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany





Benchmark of Verilog-A vs. SPICE Operating-Point Time × 10

Operating point time (seconds)		SMASH 5.15		Simulator B		Ratio	
		SPICE	Verilog-A	SPICE	Verilog-A	Verilog-A / SPICE	
	Circuit #1	0.23s	0.40s	0.02s	0.20s	10.00	
PSP Model	Circuit #2	2.17s	15.8s	0.17s	2.30s	13.53	
	Circuit #3	28.9s	6382s	2.34 s	21.17s	9.05	
EKV3 Model	Circuit #1	0.17s	0.47s	NA	0.48s	2.76	
	Circuit #2	1.22 s	90.51s	NA	5.53s	4.53	
	Circuit #3	26.3s	Too Big	NA	73.06s	2.78	



Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany







Benchmark of Verilog-A vs. SPICE Transient Speed × 15

Simulation time (seconds)		SMASH 5.15		Simulator B		Ratio
		SPICE	Verilog-A	SPICE	Verilog-A	Verilog- A / SPICE
PSP Model	Circuit #1	1.1s	17.7s	2.61s	30.1s	16.1
	Circuit #2	17.2s	249.7s	29.95s	416.8s	14.5
	Circuit #3	206.9s	3384s	284.6s	8 822s	16.4
EKV3 Model	Circuit #1	2.43 s	39.7s	NA	31.8s	13.1
	Circuit #2	31.3s	594.9s	NA	351.8s	11.2
	Circuit #3	372.7s	Too Big	NA	10 197s	27.4



Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany





Benchmark of Verilog-A vs. SPICE Summary

Verilog-A vs. SPICE	Ratio
Memory Consumption	3
Loading Time	5
Operating-Point Time	10
Transient Speed	15

The order of magnitude of the ratio is what we are looking at.

June 2010





Verilog-A Limitations Memory Consumption

Both approaches generate C code from the Verilog-A model





Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany





Verilog-A Limitations Simulation Speed

- Collapsible nodes: used, for instance, to collapse nodes when access resistances are not created.
- Bypass/linearization: for small variations, the SPICE simulator replaces the compact model by a linear model which is far faster.
- Derivation/integration: which requires one additional node.
- Specific code: at each iteration of the transient analysis, the Verilog-A simulator executes the code corresponding to the model/instance initialization, noise computation or temperature adaptation, while the SPICE simulator does not.
- Hidden states: for variables that depend on the previous point and output variables, and at each iteration of the transient analysis, the Verilog-A simulator initializes the variables with the previous value, while the SPICE simulator does not.

June 2010

Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany





Recommendations Subset of Verilog-A







Recommendations SPICE specificities

- 1. To reduce human interventions and the associated risks of having different behaviors in different simulators
 - Facilitate an efficient conversion for integration into different SPICE simulators
- 2. To reduce the memory footprint
 - Load several tens of thousands of transistors in a conventional SPICE simulator
- 3. To reduce the simulation time
 - It is of critical importance for the analog designer that the compact models run as quickly as possible in the SPICE simulator







Proposal Collapsible Nodes

- Collapsible nodes have the benefit that they reduce the size of the system matrix
 - Collapsible nodes should be defined during the instantiation phases.
 - Two ports, or one port and the ground, should not be collapsed as, in general, this will be implemented as an extra node.
- The Verilog-AMS 2.3.1 LRM does not yet specify the syntax and conditions for collapsing nodes. A commonly used "idiom" is:

```
if (r/$mfactor < 1.0e-3)
        V(a,b) <+ 0.0;
else</pre>
```

```
I(a,b) <+ V(a,b) / r;
```

• **Proposal**: use a syntax based on attributes, automatically handled during conversion of Verilog-A models into SPICE models, for instance when using ADMS XML:

```
(* collapse = "r/$mfactor < 1.0e-3" *) electrical a, b;
```





Conclusion

- For the moment, SPICE simulators remain faster than their Verilog-A counterparts.
 - Compact Models in Verilog-A should target SPICE simulators and respect the inherent constraints to facilitate their integration into different SPICE simulators
- EDA vendors will fill the performance gap between SPICE and Verilog-A simulators. Therefore, the time is coming to:
 - Make Verilog-A more attractive than SPICE for semiconductor foundries as well as for final users
 - Compete with the "Standard Model API" to address the problems of deep submicron processes such as dynamic degradation, power consumption, system-level complexity...









This work is partially supported by the European Commission FP7 under contract number 218255 (COMON).



Thanks!

MOS-AK / GSA GSA Modeling Working Group

http://www.mos-ak.org

Arbeitskreis MOS-Modelle und Parameterextraktion MOS Modeling and Parameter Extraction Working Group



COMON The Compact Modelling Network http://compactmodelling.eu



June 2010

Dolphin Integration Meylan - France Dolphin Integration GmbH Duisburg - Germany

